HCAL Electronics

H C A L

CMS HCAL ESR
Front ends and Data Links

Theresa Shaw, Julie Whitmore, Sergey Los, Scott Holm, Jordan Damgov,
John Elias, Jim Freeman, Schuichi Kunori

Outline

Front end module

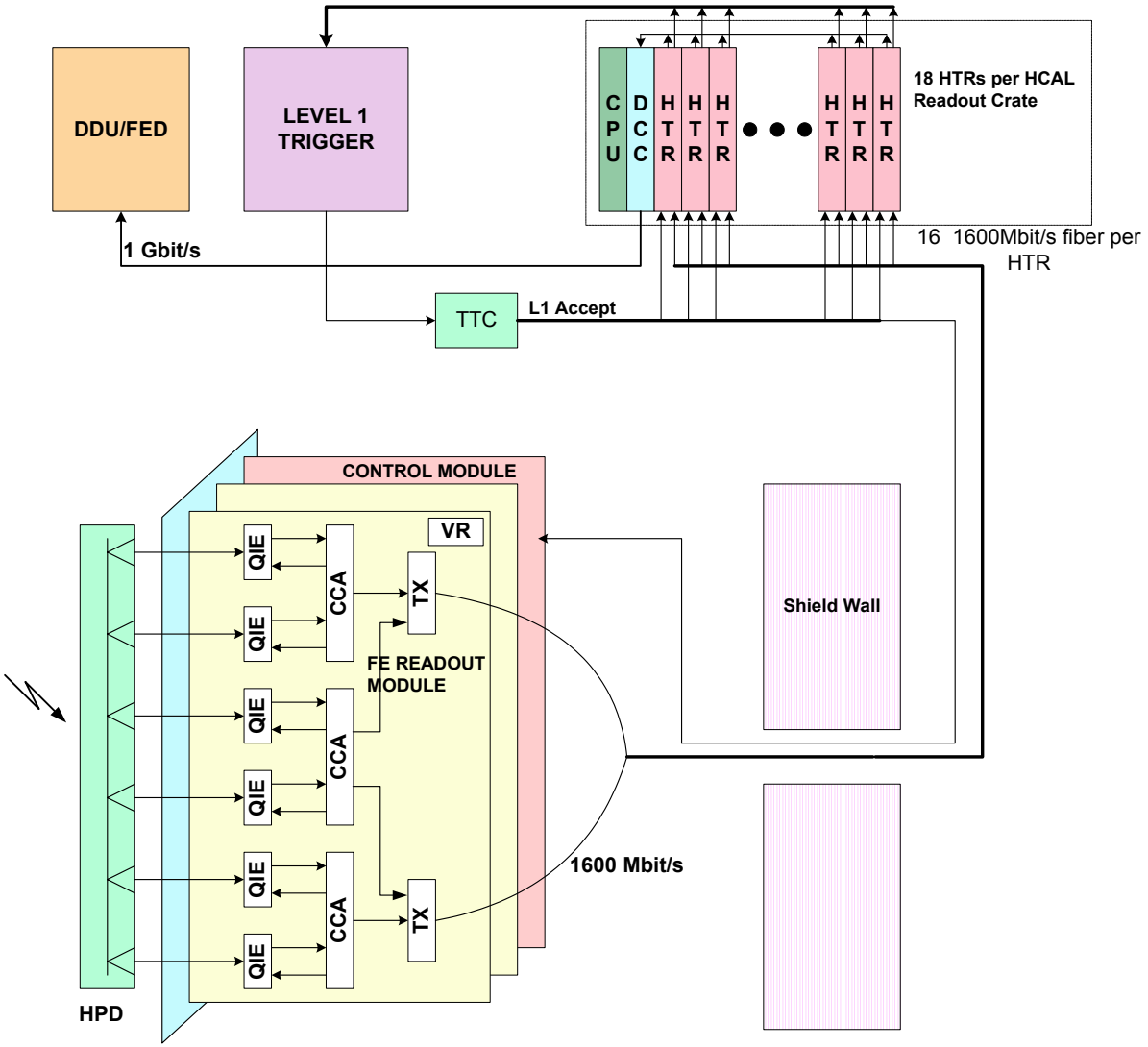
- Status
- Reset Strategy
- TB results/measurements
- Reliability tests
- Testing
- Spares
- COTS qualification
- Rad studies
- Installation plan

Clock, Control and Monitoring Module

Installation Schedule

Data links

FE/DAQ Electronics

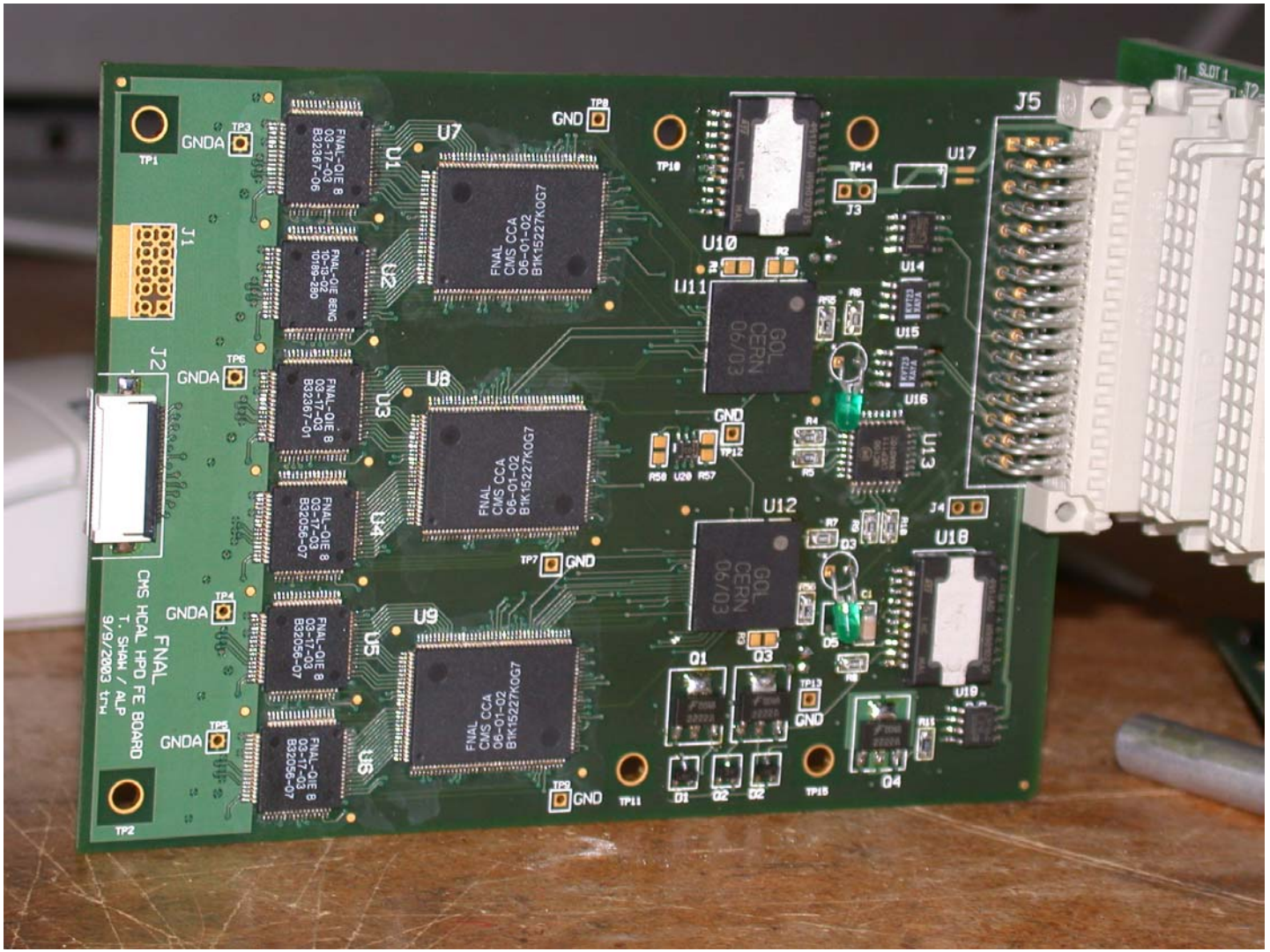


Front End Electronics

Principal components:

1. **QIE (charge integrator and encoder)**
   Fermilab ASIC -done
2. **CCA (channel control ASIC)**
   Fermilab ASIC -done
3. **GOL (gigabit optical link)**
   4200 good chips from Engineering Run wafers in hand
4. **L4913 (rad hard voltage regulator)**
   STC ASIC from CERN specifications – done
   2000 Additional parts on order
5. **HFE419X-521 (connectorized VCSEL diode)**
   Honeywell standard 2.5 Gbit/sec device – purchased
6. **All other parts in hand**
   Rad qualified

“Production” FE Card



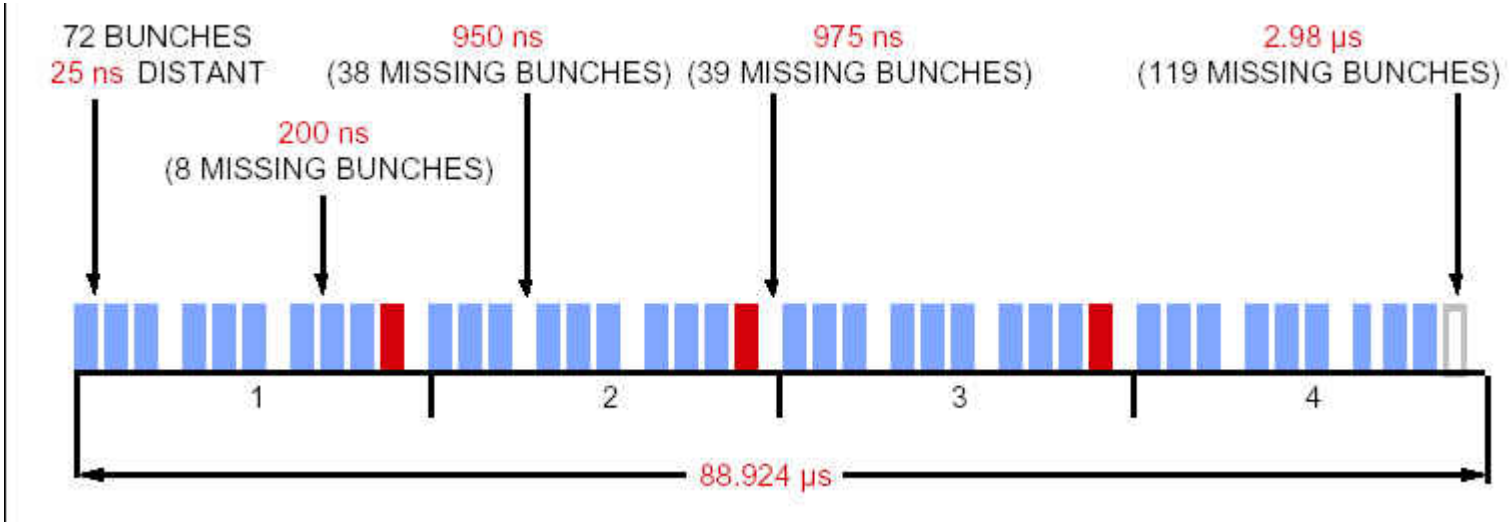
FE Module

Final version of FE Card incorporates a minor change from TB2003 module:

- "Idle" Pattern will now be sent on the Optical data link for 69 frames during the large abort gap.

Reset Strategy (1)

QIE boards are reset once per Orbit.
Reset takes place in large abort gap.
Reset function is programmable – can be turned on/off via slow controls.
Front End Reset also generates an "orbit message" on the optical data link.
Orbit message includes status word (Bunch Count value for turn) and the generation of 69 "idle" words.



Reset Strategy (2)

Resets also possible over slow controls and through TTC messaging

- **GOL/CCA Reset**
- **QIE Reset**

Testbeam 2003 Experience

Testbeam 2003 has provided valuable feedback.

QIE time slew noticed between low scale and high scale hits (on the order of 17ns)

QIE Time Slew

Contributing factors:

- **Inverting amplifier is by design slow;**

this was done to produce

  - better splitter matching
  - lower noise
- **Input impedance of the amplifier is dynamic**
  - R_{in} drops for large input currents; leading to faster response time

Bench Study QIE slew

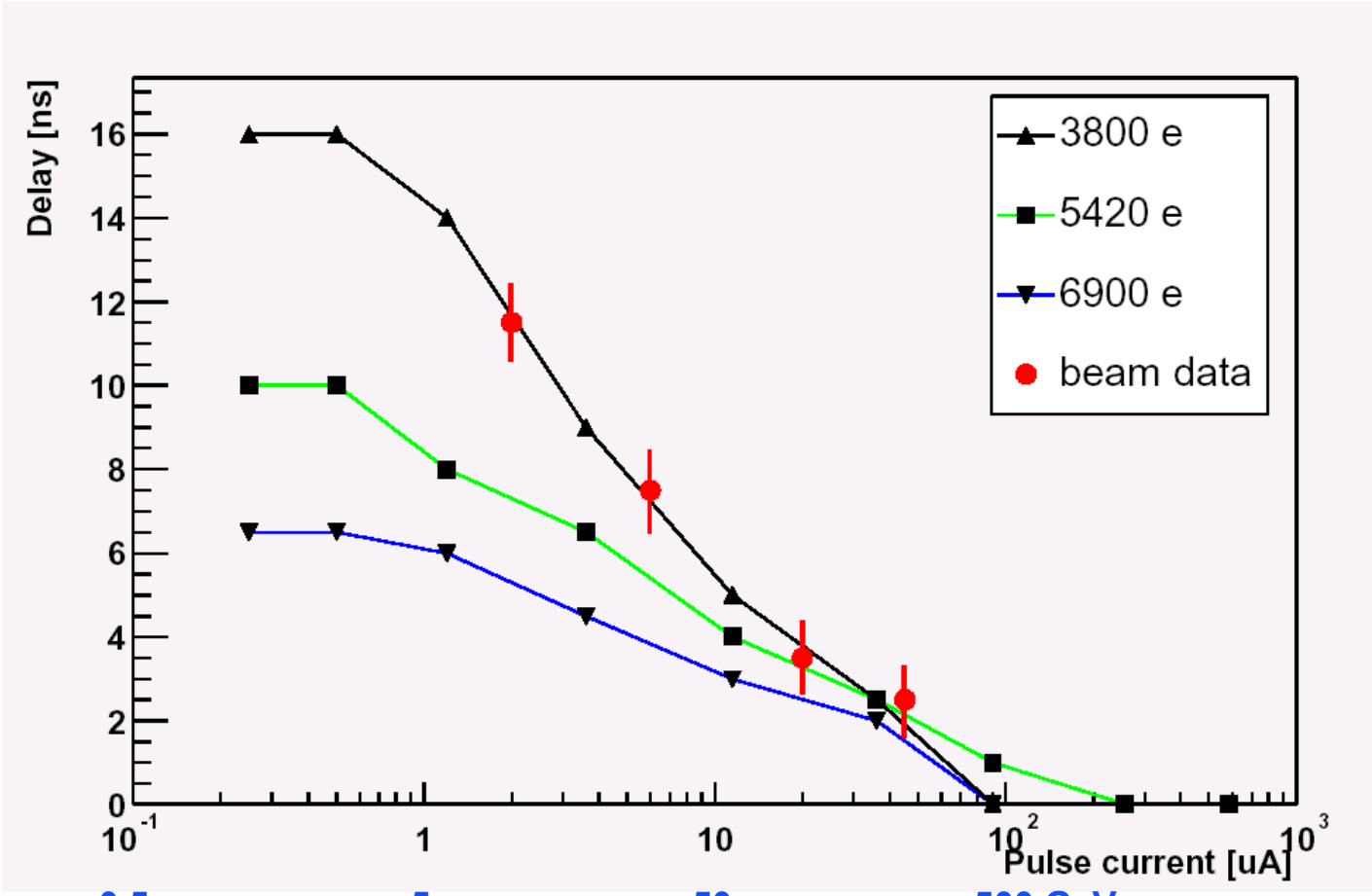
Tom Zimmerman (QIE designer) has produced a series of bench measurements of QIE response time.

Bias current of the input amplifier is selected by the value of an external input resistor.

- **Rbias = 750K (external Ibias = 4.1 uA, internal bias current = 1.03 uA) 3800e^- RMS**
- **Rbias = 304K (external Ibias = 8.3 uA, internal bias current = 2.1 uA) 5420e^- RMS**
- **Rbias = 158K (external Ibias = 13.1 uA, internal bias current = 3.3 uA) 6900e^- RMS**

Time Slew

Bench measurement and beam data



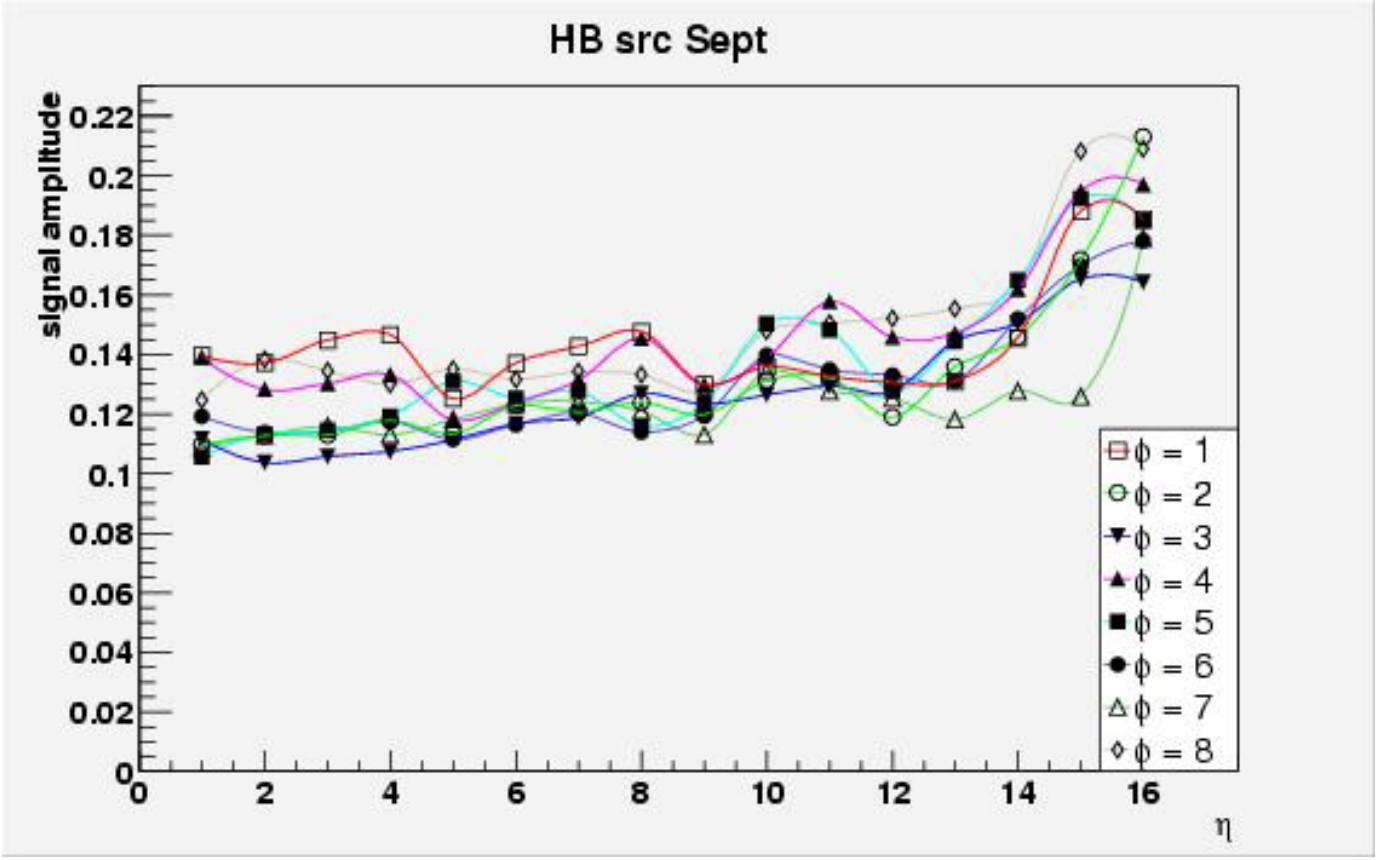
Tom Zimmerman and Jordan Damgov

QIE Sensitvity

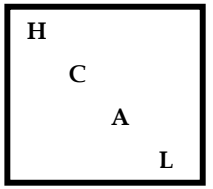
- 3 QIE chips were measured with a DAC controlled current injector in a DC mode (assumed absolute accuracy is about 2%)
- Preliminary results on the sensitivity in each of 4 ranges and their ratios are shown
- Work is in progress

QIE#	LSB in fC				R0_LSB/ CalibMode _LSB
	Range 0	Range 1	Range 2	Range 3	
1	1.060	5.31	26.8	131	2.94
2	1.123	5.59	27.5	142	2.96
3	1.074	5.32	26.0	134	3.03
RMS/ MEAN	3.1%	2.9%	2.9%	4.5%	1.5%

HB Wire Source Calibration

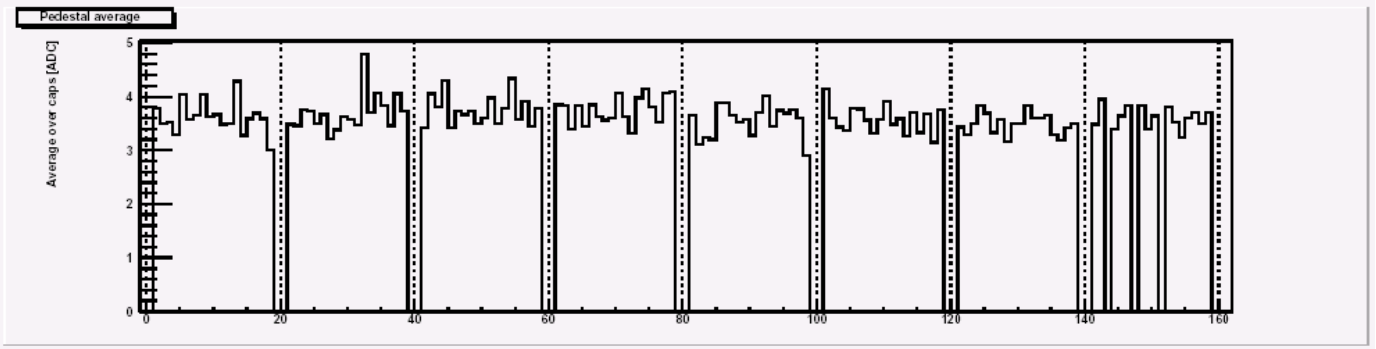


There is no big difference in the gains

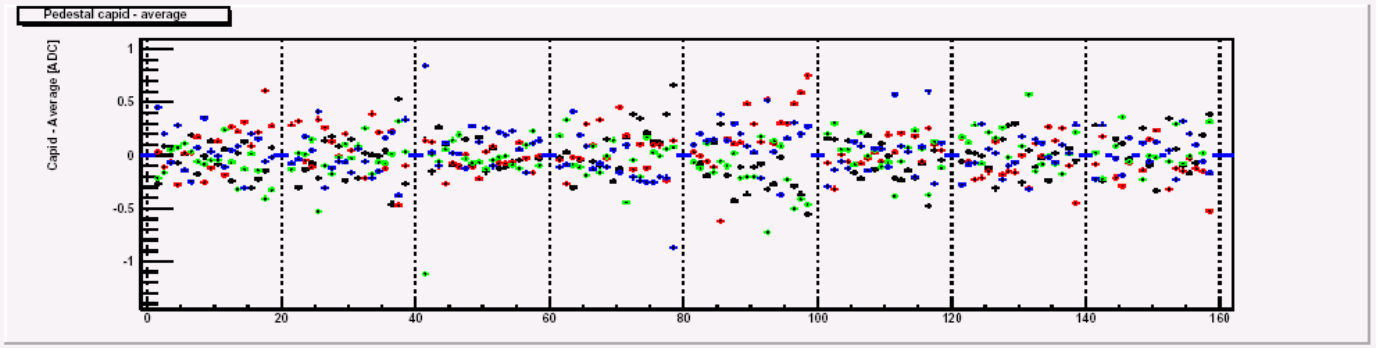


Pedestal and noise

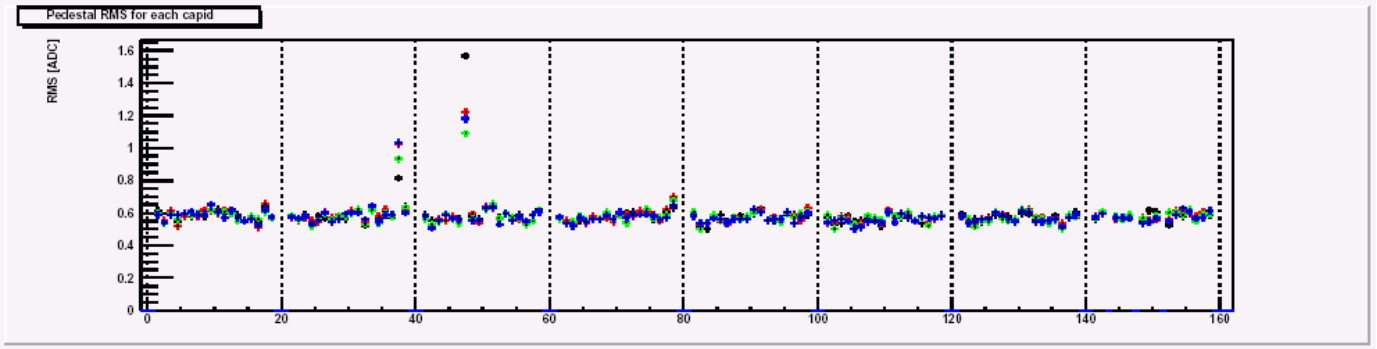
Pedestals - HB 144 channels



average



dispersion
ped(i) -ave



rms

Dynamic range

E in single HCAL readout

>3TeV jets 2.9fb → 290 events/year at 10E34.

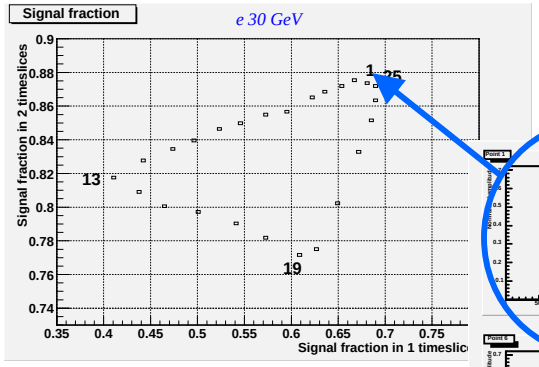
		Fraction of events above E threshold (%)					
QCD bins	MC evts	1.5TeV	2.0TeV	2.5TeV	3.0TeV	3.5TeV	4.0TeV
80-120	1000	1.40	0.60	0.30	0.00	0.00	0.00
2600-3000	2000	16.65	3.55	0.70	0.20	0.05	0.00
3000-3500	2000	28.85	7.40	1.75	0.30	0.10	0.05
3500-4000	2000	46.05	18.15	5.70	0.90	0.15	0.00
4500-5500	50	64.0	46.00	20.00	6.00	4.00	0.00

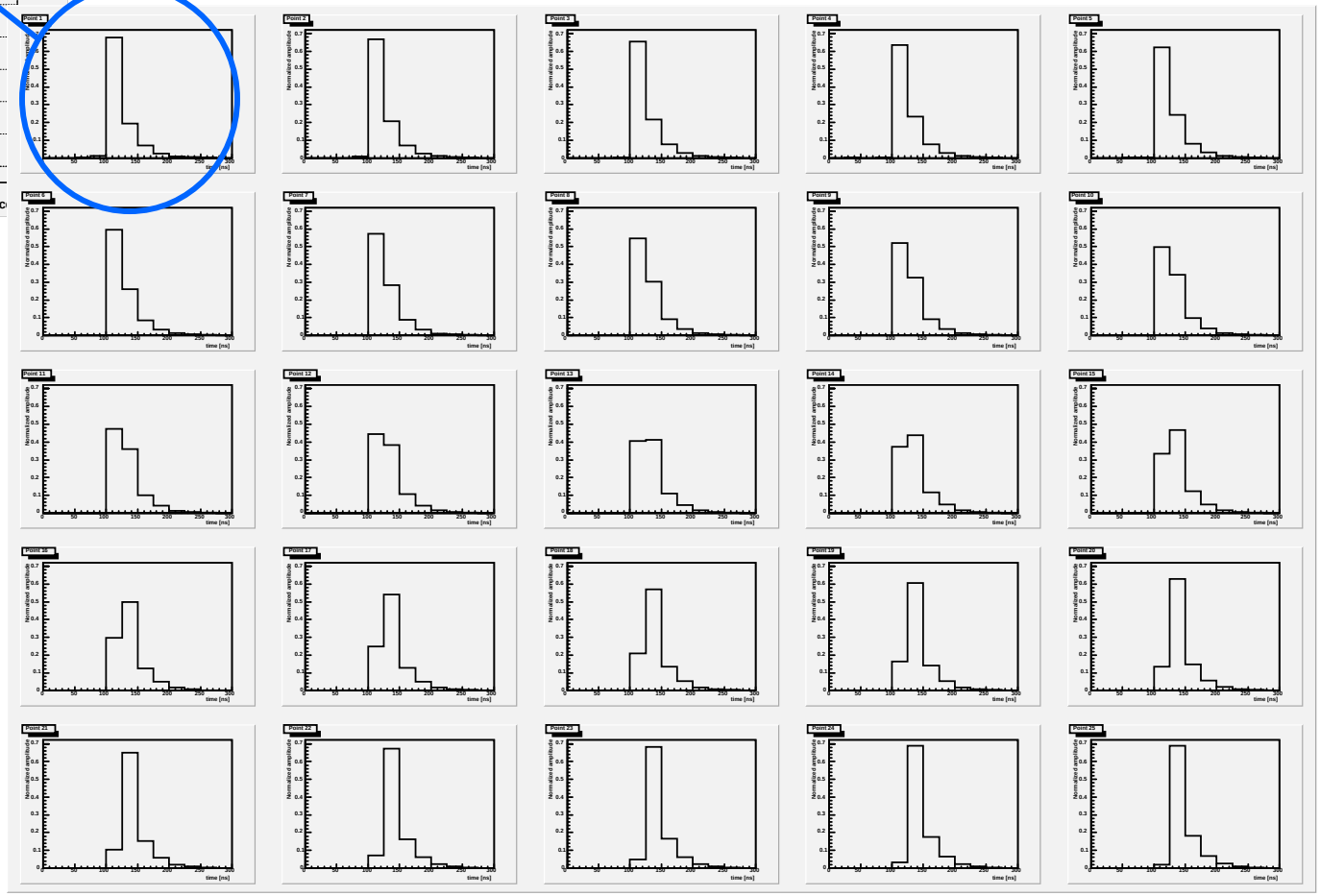
Need to cover up to 3TeV? YES.

(J.Damgov)

Pulse Shape

30 GeV Electrons





Reliability Testing Outline

- Introduction
- Reliability requirements
- Theory behind accelerated aging
- Reliability test
- Test beam experience
- Production tests
- Summary and plans

Introduction

- **We anticipate to have very limited access to the Front End crates in the HB/HO/HE areas, so electronics reliability is an important parameter.**

Reliability Requirements

Detector can produce useful data if it has

<5% of dead channels, randomly distributed.

- **Discussion is concentrated on FE electronics reliability.**
- **It is preferred not to repair electronics during the life of the detector**
- **There are several possible failure modes that we can tolerate without immediate repair:**
  - Single channel (one QIE chip)
  - Double channel (CCA chip)
  - Triple channel (serial communication)
  - Single board (CCM clock distribution, voltage regulator)
- **Failure of a whole RM opens a 5º crack in the detector and can not be tolerated**

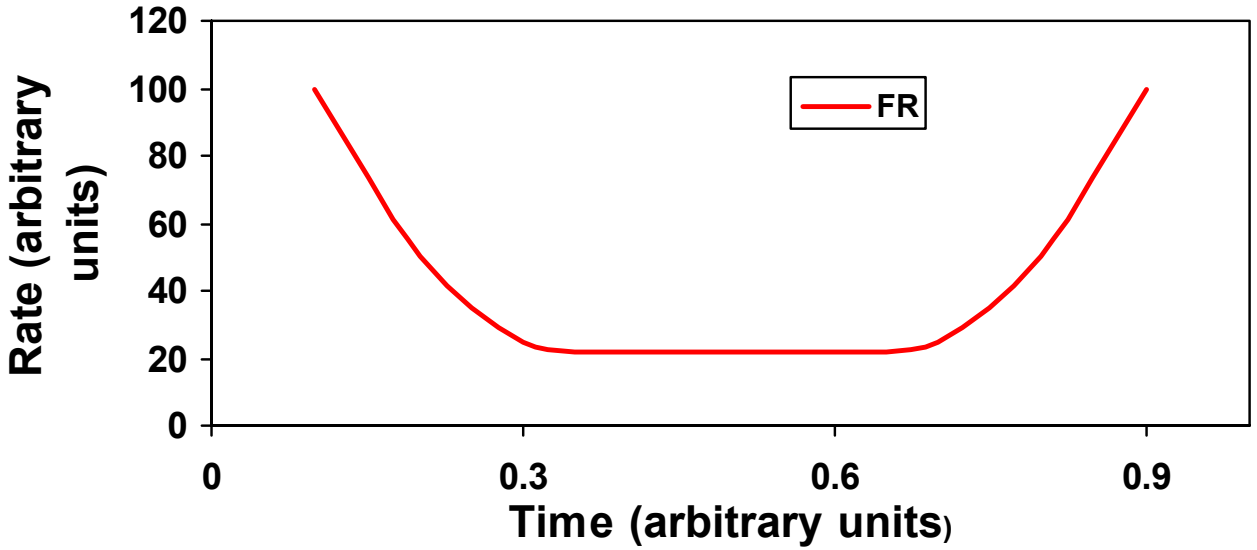
Accelerated Aging

The idea of the test is to run a subset of electronics at elevated temperature in order to get results faster.

- **Availability has limited us to a single Readout Box (RBX) for this test**
- **RBX is made of aluminum and is water-cooled, so we are using external temperature controlled recirculating water bath to control RBX temperature**
- **Equivalent time is at least 10 years (to avoid end-of-lifecycle surprises)**
- **Electronics is powered on and normally operated**
- **Periodic checking is needed to reveal dead channels (components) during the test**
  - Uses built-in LED calibration system

Failure Rate

Typical failure rate looks like that:



- "Early lifetime failure" is addressed by **Burning-in**
- "Random failure rate" and "End of life cycle" are addressed by

  Accelerated aging

Theory of Accelerated Aging

- Comes from Arrhenius law for the chemical reaction rate.

$Af=\exp(^{Ea}/_{k}(^{1}/_{T1}-^{1}/_{T2}))$

Af is an acceleration factor for two temperatures

- Problem: Activation energy is unknown!
- Solution: Extract from MIL STD-883 accelerated aging regression table (for microelectronic devices)

Answer: 0.4 eV for Burning-in

1 eV for Accelerated aging

Reliability Test

One RBX Box was subjected to an estimated 11.2 years of LHC operation so far (67 days at Af=61).

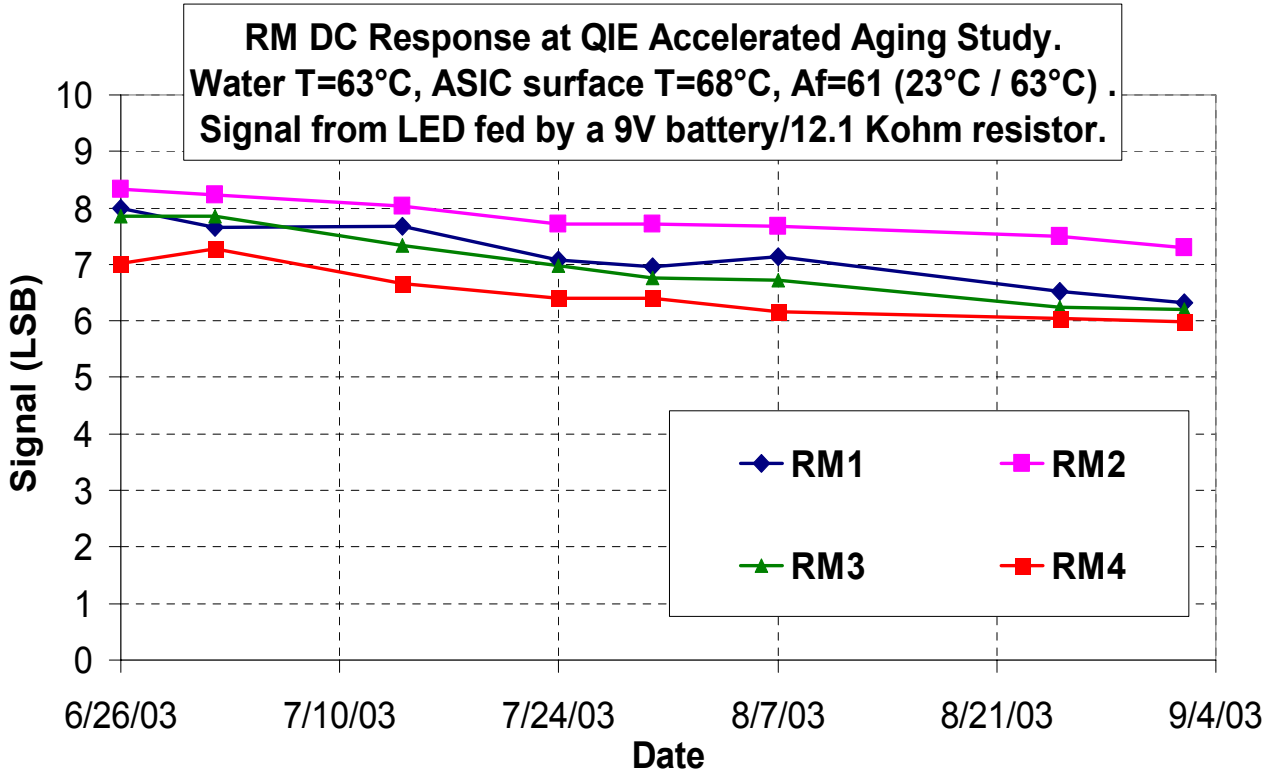
- 72 QIE (2 had problems, so we were at a 3% dead channel level at the very beginning of the test!)
- 36 CCA
- 24 GOL and VCSEL
- 24 Voltage regulators

None of the channels have failed during the test!

- Gain of each channel was monitored using a standard Calibration Module with an LED fed by an external DC current
- RMS of a pedestal distribution was another indicator of a "live" channel

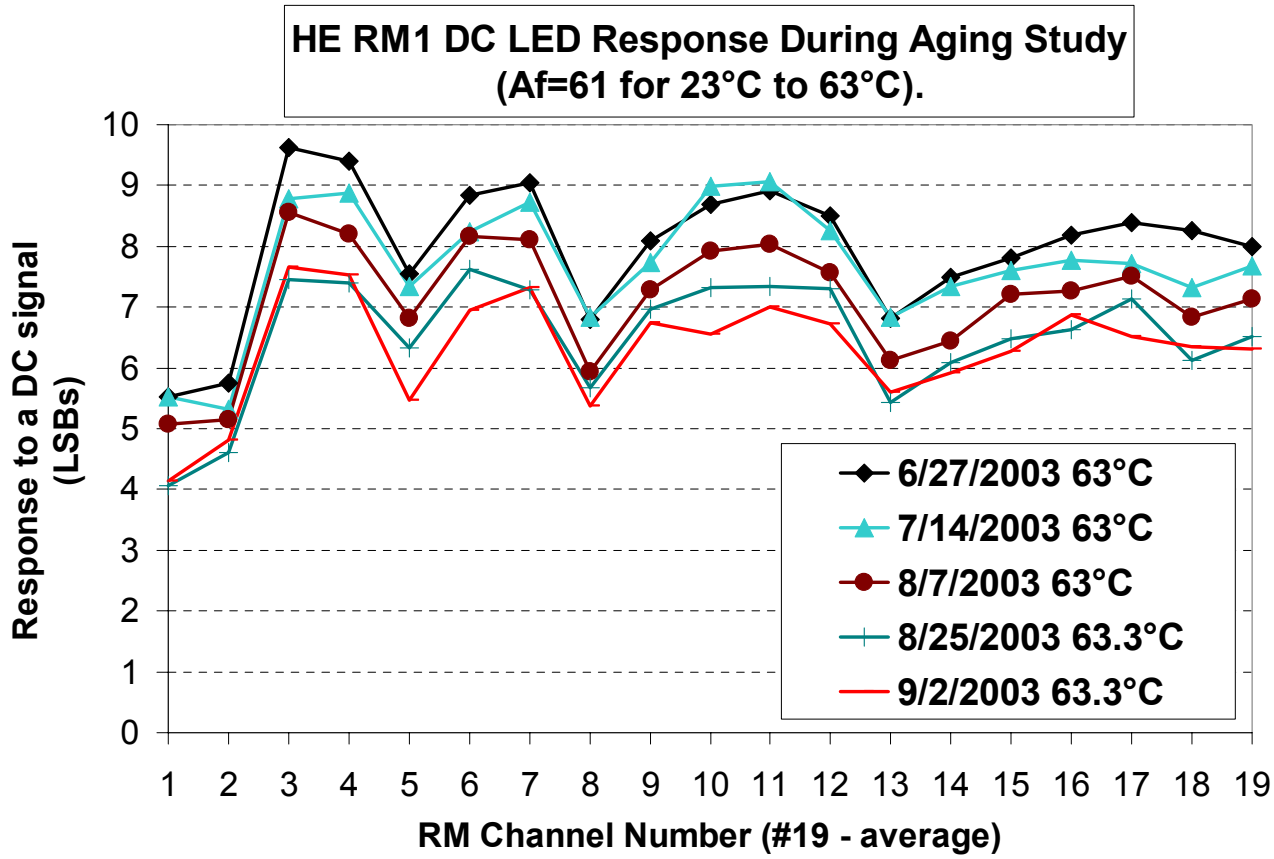
Response to a Light Source 1

- **There is a gradual decrease of response for all 4 RMs**
  - **After a 20 year aging we are planning to measure sensitivity of some of the QIE channels by direct charge injection to identify the source of the effect (QIE, HPD, LED, Fibers?)**
    - If not LED can be compensated by HV increase on HPD
    - If LED – we don't care



Response to a Light Source 2

- **Here you can see that all channels suffer from this response decrease in a more or less uniform way**
  - **Difference between the channels is determined mostly by light splitter in Calibration Module, RM3 has the same fiber mapping and the same pattern in channel response**



Test Beam Experience

2 RBXes were in operation during the 2002 test beam for 3 months

5 RBXes were in operation during the 2003 test beam for 3.5 months

Total of 2 RBX-Years

- No channel failures were observed

Reliability Results

- **No failures were observed during the test**
  - leaves us with a Poisson upper limit for average failure rate of <2.3 at 90% confidence level.
  - Given the effective number of components we have tested to 10 years we can give an upper estimate for individual component failure rate

Component	Number of parts tested to 10 years*		Max failure rate % per10y, at 90% conf. level	
	AA	AA+TB	AA	AA+TB
QIE (72/RBX)	78	92	3	2.5
CCA (36/RBX)	40	47	5.8	4.9
GOL(24/RBX)	27	32	8.3	7.2
VReg(24/RBX)	27	32	8.3	7.2

* - (parts×years/10years)

AA – Accelerated aging, TB – Test beam data

Production Tests

QIE Boards

- All cards will go through 5-10 thermal cycles (20-70°C) without power
- Burn-in test will include 1 week at normal operating temperature (before installation on the detector in SX5)
- Additional burn-in/commissioning at SX5 for a minimum of 4-6 weeks

Testing Scenario

All ASICs are individually tested before being mounted on cards.

FE cards are tested individually and assembled into three card packs prior to insertion into the Readout Modules (RMs).

RMs (including FE electronics) are tested within an RBX, left powered and clocked for a week, and re-tested.

RMs and RBXs are shipped to CERN and tested prior to installation on the detector.

RMs and RBXs are re-tested following installation.

Plan for Spares

There will be 20% spares built for all FE modules.

In addition, we will stock 40% spare parts of all ASICs and 20% of all commercial parts.

RBX Cooling

- RBX power dissipation ~80 watts
- 1 Liter/minute flow rate resulted in 1^0 C delta T.
- Plan is to supply 1 l/min flow at ~20^0 C.
- Delta T chip surface to water temp measured to be 5 degrees C (?? Check)
- Chip operating temp should be less than 30 degrees C.
- A Delta-T of 5 degrees C is acceptable
- → easily factor of 5 in cooling
- N.b. If the water is turned off completely, measured delta T of RBX was 5^0 C

RBX Cooling

- RBX power dissipation ~80 watts
- 1 Liter/minute flow rate resulted in 1^0 C delta T of coolant.
- Plan is to supply 1 l/min flow at ~20^0 C.
- Delta T chip surface to water temp measured to be 5 degrees C
- Delta T die-package surface for QIE (for example) calculated to be 30C. (10^0C/watt * 0.3 watts)
- QIE die temperature therefore is ~ 20 + 5 + 3 = 28^0C
- Very conservative goal is that the die operating temp should be less than 40 degrees C.
- A Delta-T of 10 degrees C of the coolant is acceptable
- → easily factor of 10 in cooling
- N.b. If the water is turned off completely, measured delta T of RBX was 5^0 C

HV Reliability Pre-production Study

For a HV cable/distribution chain failure of a single component takes out a full 5º sector out of operation

- There is a spare HV wire in every cable that we can use to bypass a damaged one without recabling
- Two HV Units have been exposed to 50 thermal cycles from +25 to +105°C with no deterioration in leakage current
- The same HV Units have undergone an accelerated aging test

HV Accelerated Aging

HV study

- HV cable + HV unit – monitored for increased leakage at 18 kV (12 kV operating voltage) during a 15 year equivalent aging test at 80°C (4 months) while being stressed at a 25 mm bending radius.
- Small decrease in leakage current seen due to bake-out
- the integration group has found routing from the splice box to the RBX locations that complies with the Kerpen data sheet recommendation
- one unavoidable tight bend remains just at the entry to the HE RBX

COTS Qualification

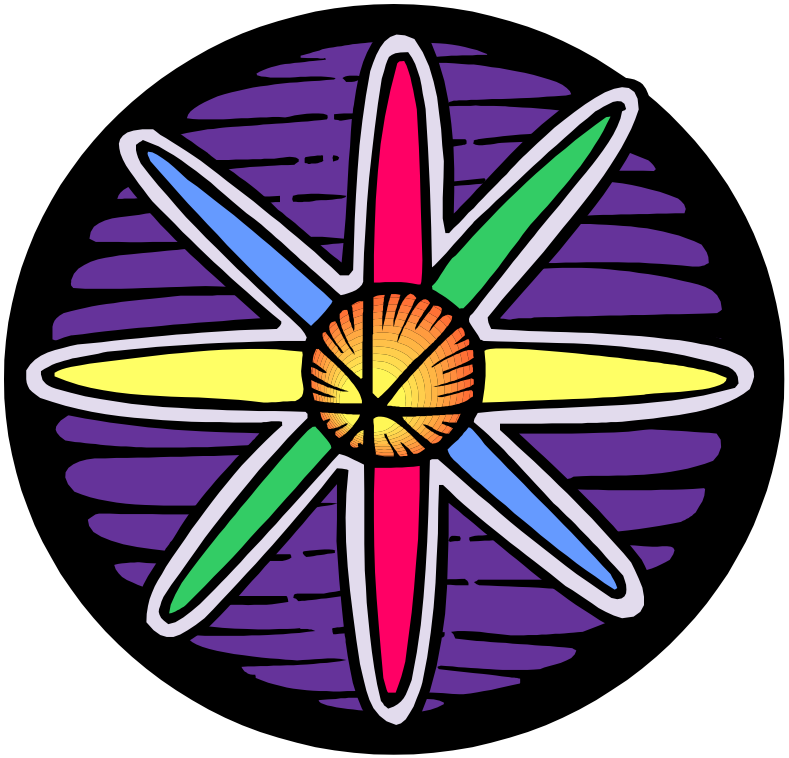
All production parts were made or purchased from a single fabrication lot.

Cards were made in Spring'03 with these production parts.

These cards were used in the

- Reliability Test
- Rad Qual Test

Radiation Tolerance Studies



FE Board

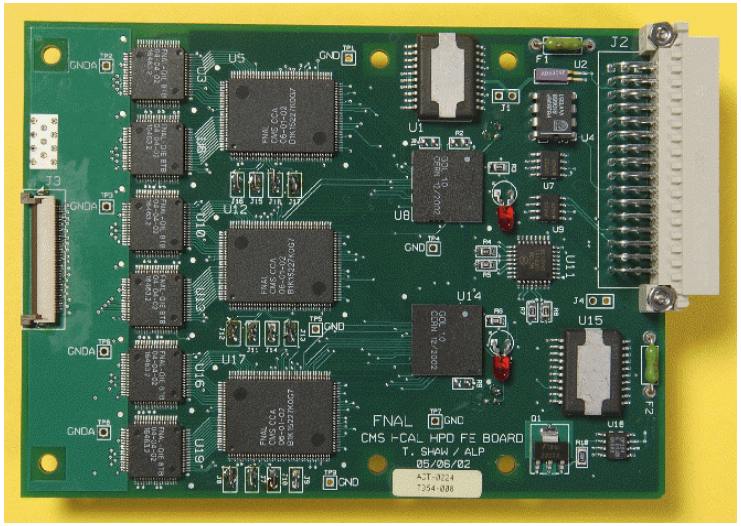
Test FE boards for latchup (1644 boards in system)

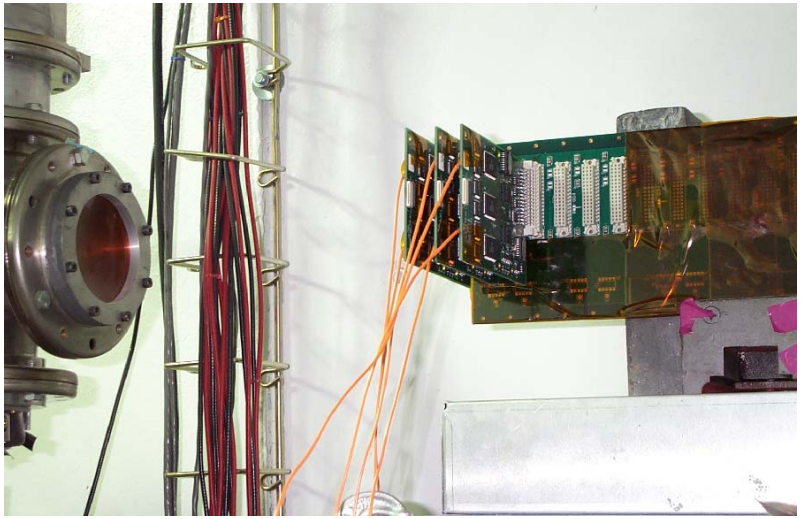
- **18 boards tested – Total fluence=10yr dose for full system (1.27E14 p/cm^2)**
  - No latch-ups seen – Used overcurrent circuit on board and GPIB monitoring of LV supply
    - **6.5V supply draws lots of current due to CMOS section of QIE failing from TID. Seen in previous shift register test. However, no true latch-ups.**
  - FE boards are latch-up immune to 10yr level for full system

FE Board Testing Procedure

Testing Strategy

- **Qualified all FE components to 10yr level for system**
- **FE boards**
  - Dosed 2 boards for SEL and crude SEU study and 15 boards for SEL and SEU study (full DAQ readout)
  - Beam spot focused on QIE and CCA section of board (GOL and LV regulators assumed rad tolerant)

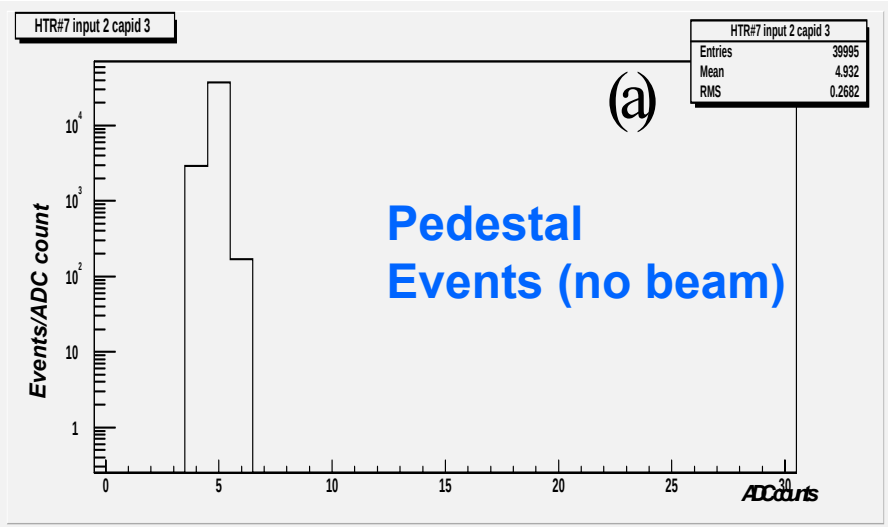


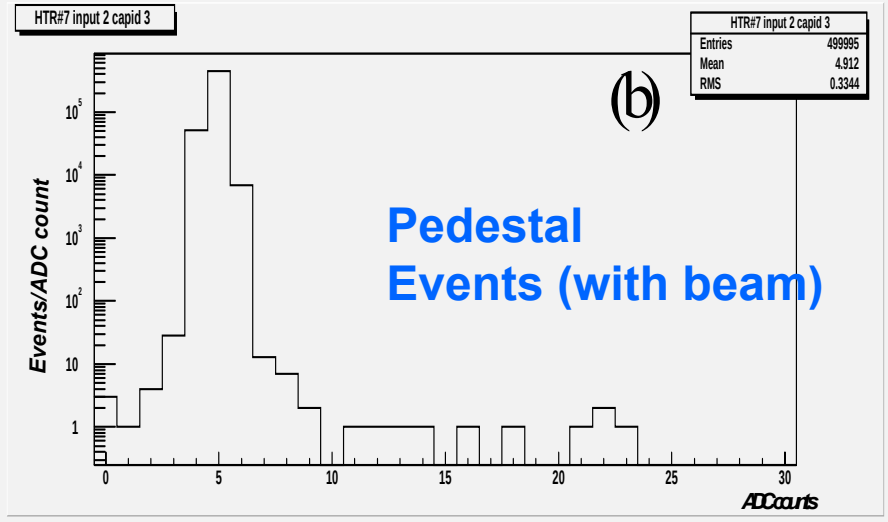


FE Board Test

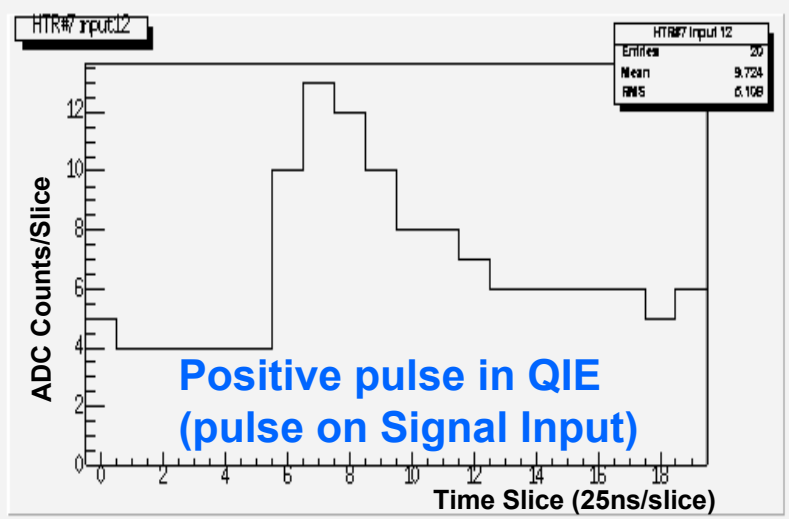
FE Board response in 200 MeV proton beam

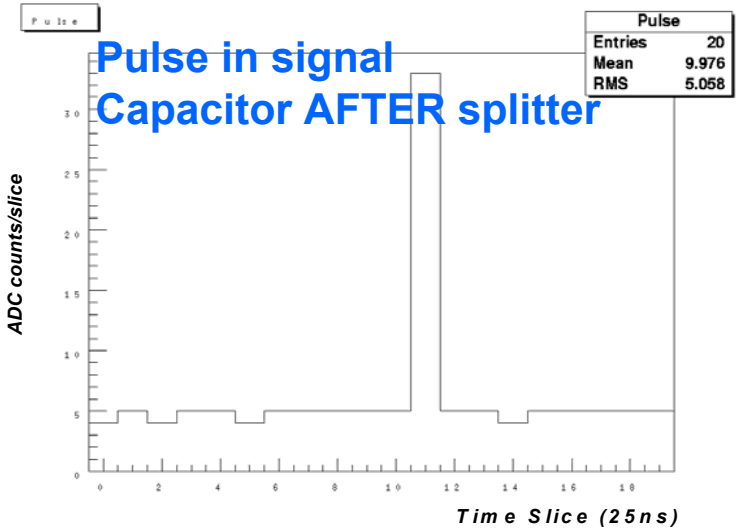
- **Several pathologies**
  - Signals in QIE in front of integration caps (signal & reference)
  - Signals in QIE on back of end caps (signal follows cap)
  - SEU events

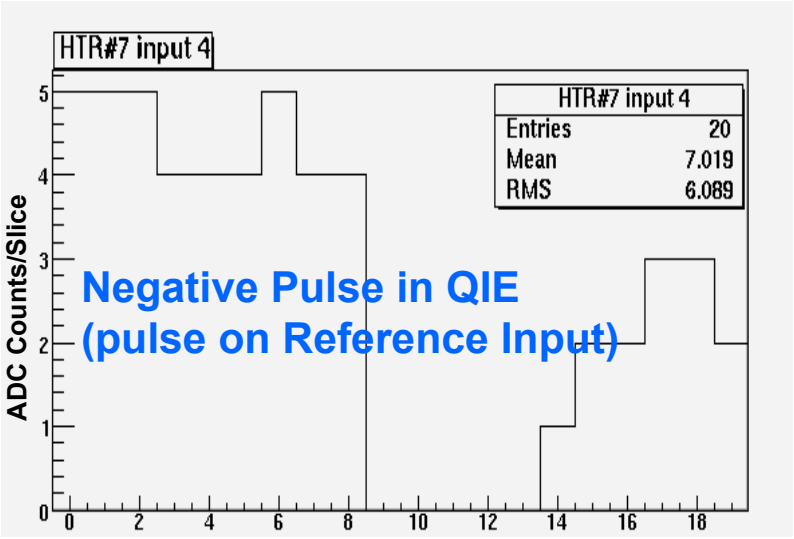




FE Rad Data Pathologies







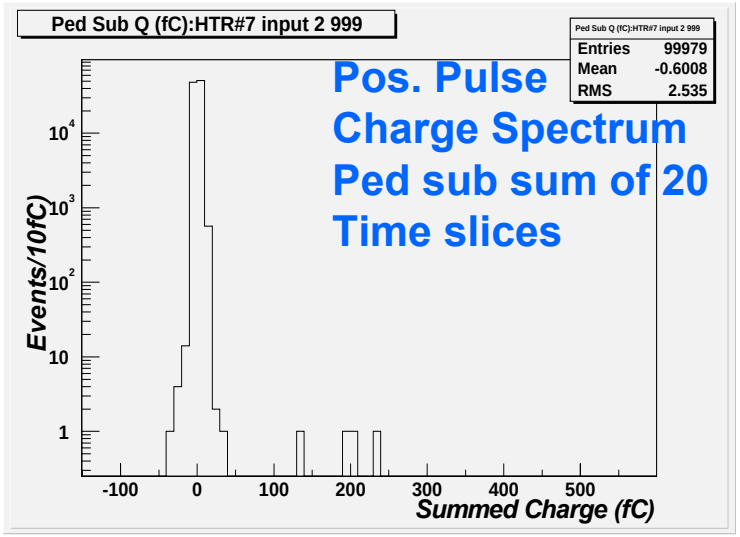
Protons Interacting in QIE

Pulses in QIE silicon

- Spectrum depends on active volume of QIE – difficult to calculate
- Same phenomenon as seen in HPD radiation test
  - MIP in Si (48k e^- ~ 8fC) per 300 μm
  - Inelastic nuclear int. ~ 1pC (only 1% of interactions)
- In the QIE, the highest energy events were 250-500fC
  - Time profile slower than detector signals

HCAL implications

- Rate of the high energy QIE interactions will be ~20 events/QIE/year



FE Board SEU Studies

SEU Xsec Results

- **Need to separate proton interaction in Si events from true SEU**
  - Special runs taken with Multi-range ADC (QIE) put into higher ranges ["Forced Range" (Range 2&3)]
  - Energy deposition from proton interaction in Si too small to shift pedestal
- **SEU special runs – Fixed range runs: No SEU seen after 5.8E13 p/cm^2 → Xsec limit of <1.7E-14cm^2 for a board**
- **But SEU measurement is limited by data rate**
  - Rad test trigger rate (125Hz ~ 1% expected CMS L1 trigger rate) → Upper limit * 100
- **Best limit: 1.7E-12cm^2 → Expected # SEU in HCAL system < 21.8 SEU/yr**
  - (ASIC shift register studies predicted 15-30 upsets/yr)
    - **QIE – ~15 cells, only 1 is SEU tolerant**
    - **CCA – all cells designed to be SEU tolerant**

GOL Studies

GOL-SEU/SEL/Lockup

- GOL study conducted to investigate possible lock-up
- 6-channel front-end boards – 14 boards
  - Beam focused on GOL, LV regulators, clocking chips
  - 2 GOL/board-Old and new GOLs studied
  - 1.6Gbps, 8B/10B
- Boards continuously read out. Scope set to trigger on Frame Errors and Data Valid Errors
- Total fluence: 1.68E14 p/cm^2

SEL

- No SEL seen → No SEL expected in full system/10yrs operation

Lock-ups

- No lock-ups seen → No lock-ups expected in full system/10yrs op.

SEU X-section

- (2.3-3.8)E-13 cm^2
- Expected SEU rate: 3.9 SEU in system/yr operation

CCM

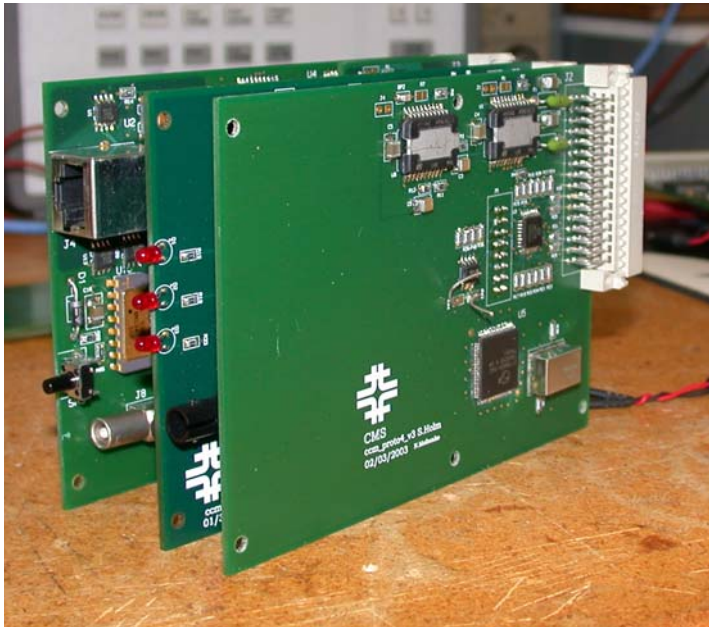
Test CCM for latch-up (132 modules in system)

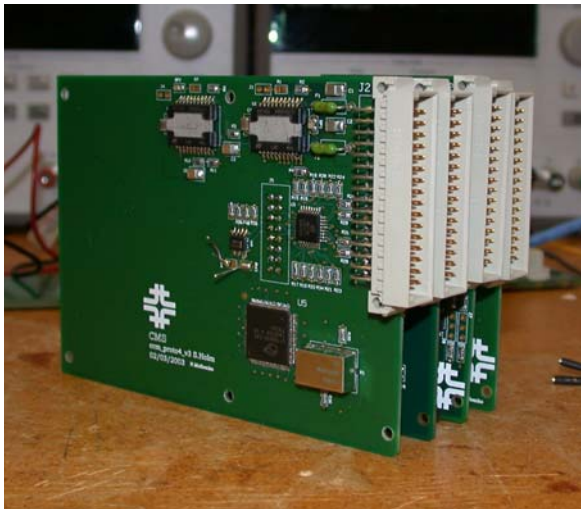
- **Write/read registers continuously during irradiation**
- **1 board – Fluence = 25 x 10yr dose for 1 board**
  - No read errors & no latch-ups seen Overcurrent circuit trips at ~2.5E12 p/cm^2 (~150 kRad)
  - A/D stops working → Actel part stops working
    - **No triple module redundancy (TMR) in Actel part**
    - **Actel with TMR operates error-free for 4.7E12 p/cm^2**
  - Set limit of < 1 SEL /2yrs operation
  - Need ~5 boards to study SEU/SEL in CCM system for full 10yr operation
    - **Plan to conduct test ~Winter 2003.**

Radiation Validation Status & Plans

- **All components tested and validated** (FERMILAB-CONF-02-224-E & FERMILAB-CONF-01-250-E)
  - All components operate well beyond 10yr dose levels
  - SEL limit of < 1 SEL / 10yr for FE system and < 1 SEL / 10yr for CCM system achieved for each component
  - Set limit of <<1 SEB / 10yr for HPDs
  - Developed methodology for de-rating of input voltage, output voltage and output current
    - **No SEBs seen when operated in appropriate de-rated conditions**
- **SEU/SEL test conducted on FE boards and SEU/SEL/Lockup tests conducted on GOL/LV reg.** (FERMILAB-CONF-03-316-E)
  - SEL immune to 10yr level for full system
  - Lockup immune to 10yr level for full system
  - SEU looks to be at a tolerable level
    - **Total rate:<25.7 SEU/yr for full system**
  - Proton interactions in Si (ASICs & HPD)
- **HCAL FE electronics production to begin Autumn `03**

Clock, Control and Monitor Module



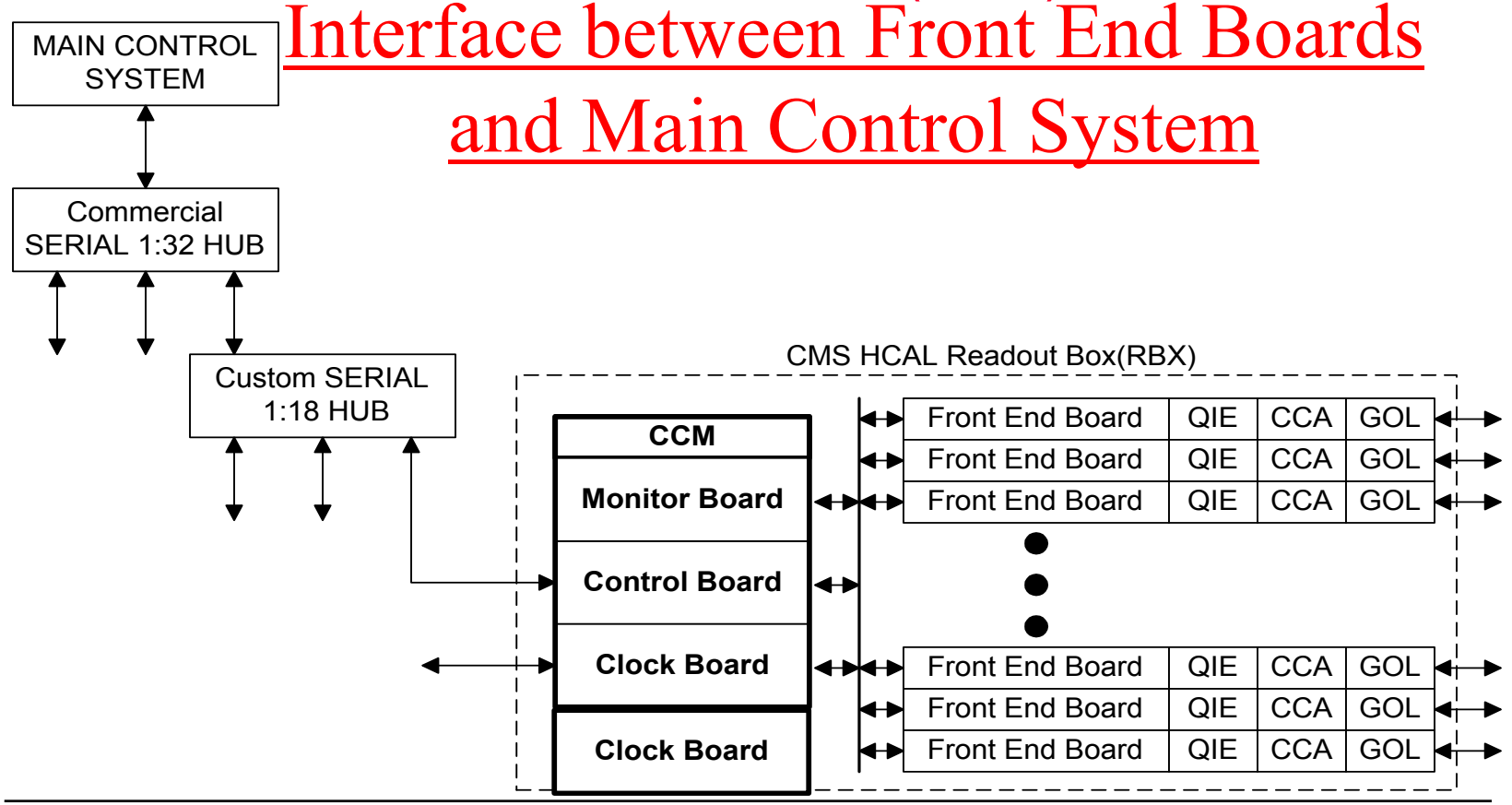


CMS HCAL TIMING & CONTROL MODULE(CCM)

CCM "CLOCK – CONTROL – MONITOR"

CCM - FOUR Board Module that resides in the CMS HCAL Readout Box(RBX)

Interface between Front End Boards and Main Control System



STATUS

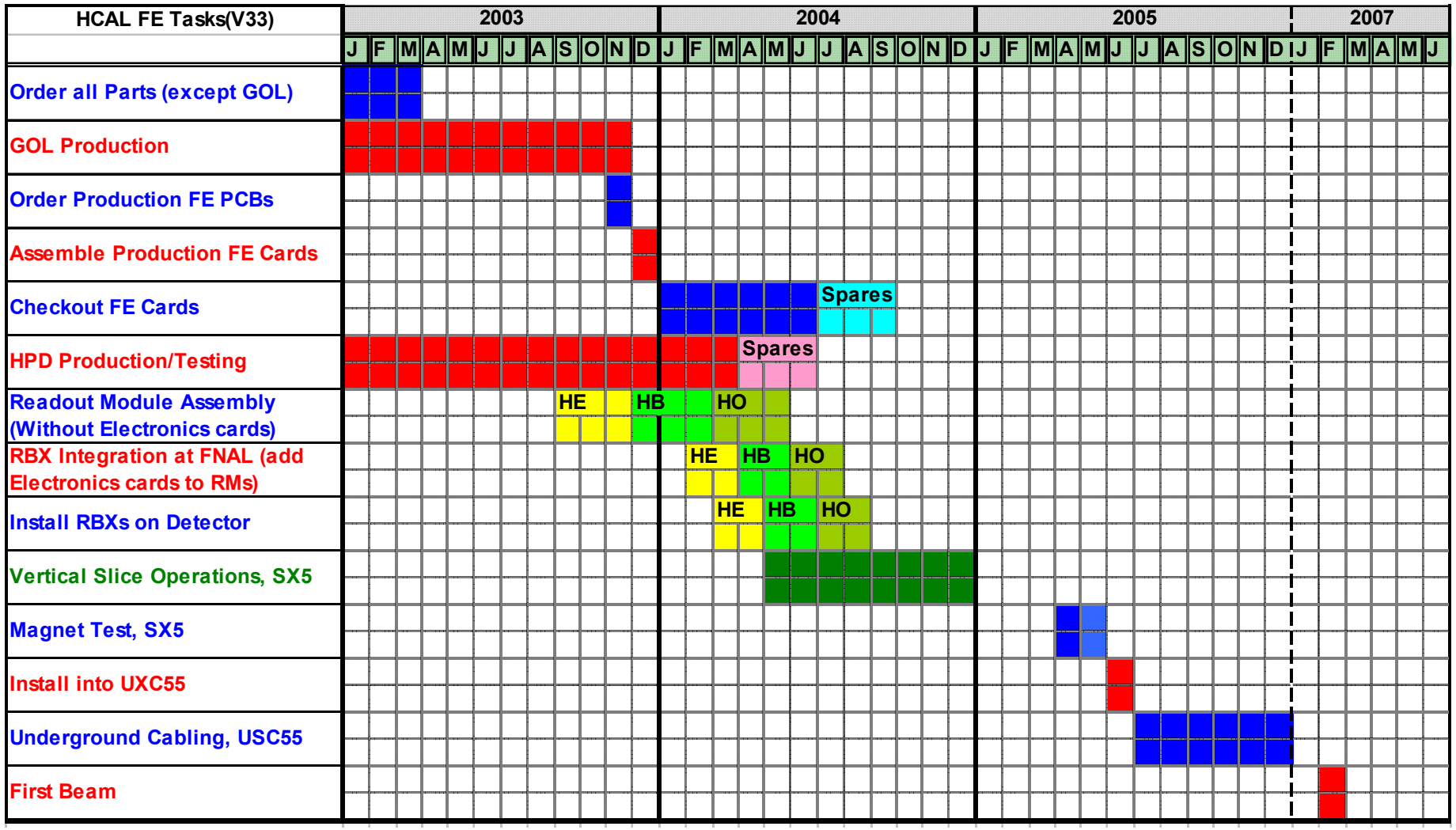
- V2 Modules used in Test Beam 2003
- Serial Interface & Communication software exercised in TB-2003 & TB-2002
- FPGA Design(Controller Board)
  - Design placed in Actel Antifuse part – tested(40% of FF cells used). Modified design using TMR strategy simulated(90% of FF cells used).
- Mechanical Module Design & Fabrication
  - Dependent upon layout of next version of board.
  - Similar Scheme to Front End cards.
- 2 Looming design changes

CMS HCAL TIMING & CONTROL MODULE(CCM)

- Changes Done
  1. **Add QPLL to clock circuitry (prototyped).**
  2. **Turn off clock to backplane(FE boards) during POR and during a reset (prototyped).**

- Future Changes
  1. **Add High Speed connector between clock boards.**
  2. **Change Monitor board size for mechanical reasons.**
  3. **Change ACTEL FPGA to newer – larger part**

HCAL FE Production Schedule



Summary

Steady Progress

- QIE development/bench studies – begin 1999
- 2 channel card – June ‘01
- 2 channel card w/HPD – Aug ‘01
- 6 channel card w/HPD – March ’02
- 144 Channels in the test beam – Aug ’02
- 200 Pre-prod cards built Feb/Mar’03
- 10 “Prod” cards built Oct’03

HCAL Opto-link Overview

Design requirements

- **~3000 data + TTC/calibration links**
- **High-speed digital operation - 1.6 Gbps**
  - 3 channels/link – reduce cost
- **Radiation tolerant**
  - TID: 1kRad and neutron fluence: 4E11 n/cm^2
- **Small form factor**
  - Tight space constraint at RBX and HTR front-panel
- **Achieve layer-tower channel mapping**
- **Need to pre-cable HE → Patch panel**

VCSEL Selection

Honeywell

Fiber Optic LAN Components HFE419x-541

LC Connectorized High Speed VCSEL 2.5 Gbps

FEATURES

- Designed for small form factor transceivers
- Prealigned connector sleeve that is compatible with the LC standard (LC is a trademark of Lucent Technologies)
- Designed for drive currents
- Optimized for low dependence of electrical properties over temperature
- High speed ≥1 GHz
- Two different laser/ photodiode polarities
- Attenuating coating
- Packaged with a photodetector

The HFE419x-541 is a high-performance 850 nm VCSEL (Vertical Cavity Surface-Emitting Laser) packaged for high-speed data communications. This product combines all the performance advantages of the VCSEL with a custom designed power monitor diode. The power monitor diode can be used with appropriate feedback control circuitry to set a maximum power level for each VCSEL. In addition, built-in power attenuation reduces the effective slope efficiency. These combined features simplify design for high data rate communication and eye safety.

Packaged in a fiber receptacle sleeve, this high radiance VCSEL is designed to convert electrical current into optical power that can be used in fiber optic communications and other applications. As the current varies above threshold, the light intensity increases proportionally.

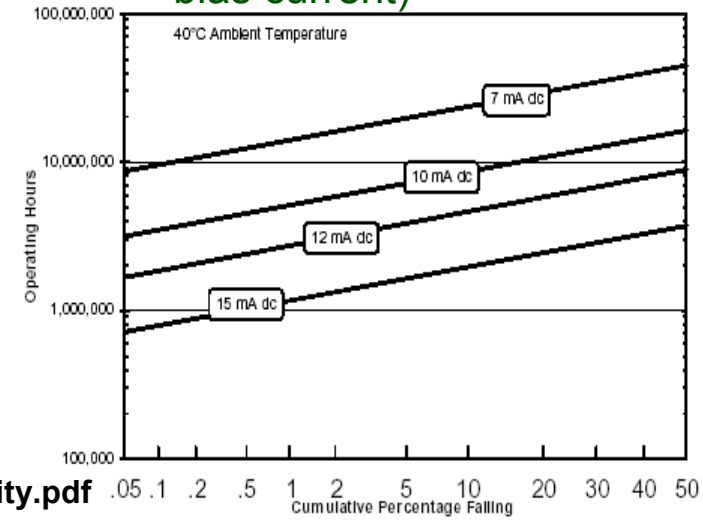
The HFE419x-541 is designed to be used with inexpensive silicon or gallium arsenide detectors, but excellent performance can also be achieved with some indium gallium arsenide detectors.

The low drive current requirement makes direct drive from PECL (Positive Emitter Coupled Logic) or EML (Emitter Coupled Logic) gates possible and eases driver design.

The HFE419x-541 is a prealigned and focused fiber optic transmitter designed to interface with 50/125 and 62.5/125 µm multimode fiber.

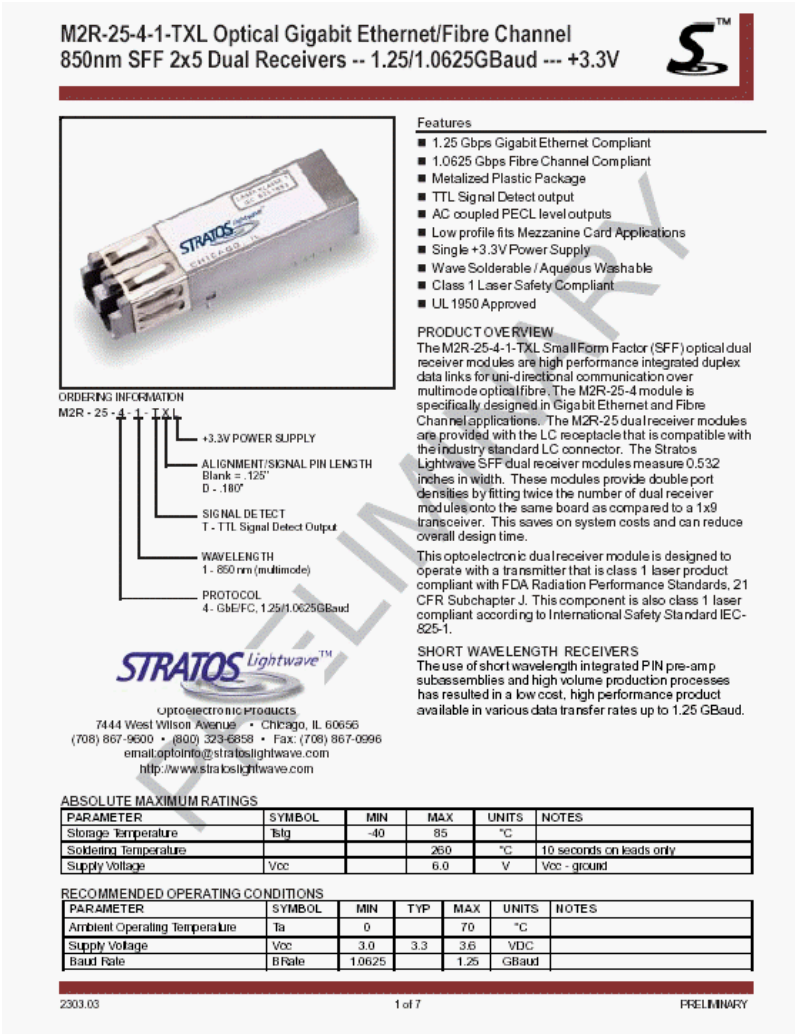
Honeywell VCSEL

- High speed operation (2.5 Gbps)
- Operated well in test beam
- Radiation tolerant
- Good reliability
  - No sig. infant mortality
  - Only wear-out failures (10yrs = 88k hrs, <7mA bias current)



http://www-ppd.fnal.gov/tshaw.myweb/CMS/Parts/VCSEL_reliability.pdf

Receiver Selection



M2R-25-4-1-TXL Optical Gigabit Ethernet/Fibre Channel
850nm SFF 2x5 Dual Receivers -- 1.25/1.0625GBaud --- +3.3V

Features
- 1.25 Gbps Gigabit Ethernet Compliant
- 1.0625 Gbps Fibre Channel Compliant
- Metalized Plastic Package
- TTL Signal Detect output
- AC coupled PECL level outputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

ORDERING INFORMATION
M2R - 25 - 4 - 1 - TXL
- +3.3V POWER SUPPLY
- ALIGNMENT/SIGNAL PIN LENGTH: Blank = .125", D - .180"
- SIGNAL DETECT: T - TTL Signal Detect Output
- WAVELENGTH: 1 - 850 nm (multimode)
- PROTOCOL: 4 - GbE/FC, 1.25/1.0625GBaud

PRODUCT OVERVIEW
The M2R-25-4-1-TXL Small Form Factor (SFF) optical dual receiver modules are high performance integrated duplex data links for uni-directional communication over multimode optical fibre. The M2R-25-4 module is specifically designed in Gigabit Ethernet and Fibre Channel applications. The M2R-25 dual receiver modules are provided with the LC receptacle that is compatible with the industry standard LC connector. The Stratos Lightwave SFF dual receiver modules measure 0.532 inches in width. These modules provide double port densities by fitting twice the number of dual receiver modules onto the same board as compared to a 1x9 transceiver. This saves on system costs and can reduce overall design time.

This optoelectronic dual receiver module is designed to operate with a transmitter that is class 1 laser product compliant with FDA Radiation Performance Standards, 21 CFR Subchapter J. This component is also class 1 laser compliant according to International Safety Standard IEC-825-1.

SHORT WAVELENGTH RECEIVERS
The use of short wavelength integrated PIN pre-amp subassemblies and high volume production processes has resulted in a low cost, high performance product available in various data transfer rates up to 1.25 GBaud.

STRATOS Lightwave™
Optoelectronic Products
7444 West Wilson Avenue • Chicago, IL 60656
(708) 867-9600 • (800) 323-6858 • Fax: (708) 867-0996
email:optoinfo@stratoslightwave.com
http://www.stratoslightwave.com

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Storage Temperature	Tstg	-40	85	°C	
Soldering Temperature			260	°C	10 seconds on leads only
Supply Voltage	Vcc		6.0	V	Vcc - ground

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	Ta	0		70	°C	
Supply Voltage	Vcc	3.0	3.3	3.6	VDC	
Baud Rate	B Rate	1.0625		1.25	GBaud	

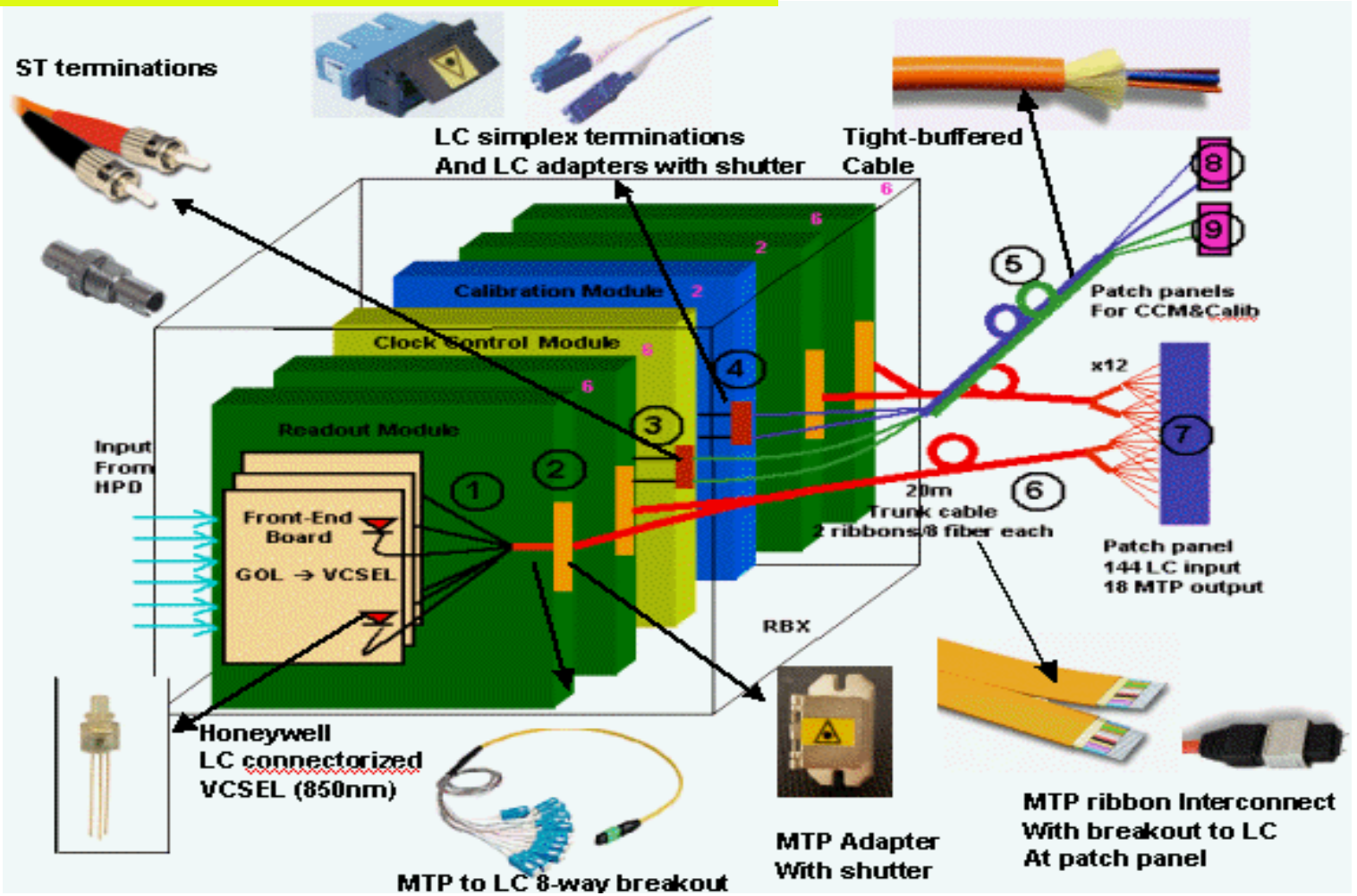
2303.03 1 of 7 PRELIMINARY

Dual receivers at HTR

- Stratos M2R-25-9-1TL transceiver → Texas Instruments TLK2501 deserializer (1.5-2.5 Gbps operation)

HB/HE/HO Design (1)

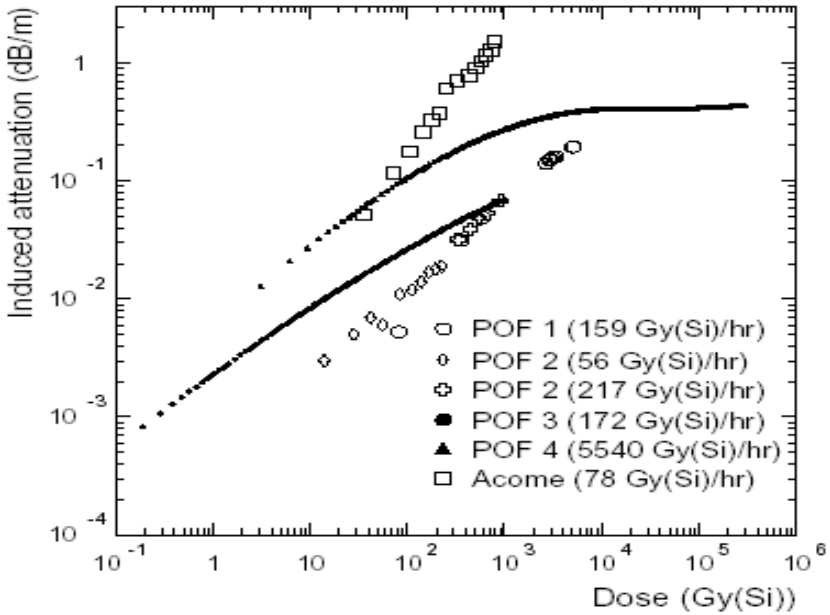
1.6 Gbps Digital Readout
~3500 Data + TTC/Calibration Links



Cable

Cable requirements

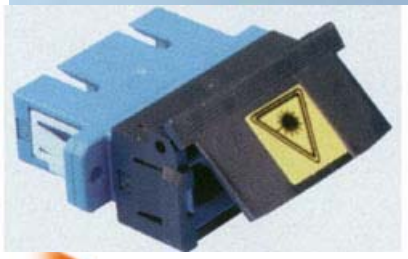
- **Able to transmit 1.6 Gbps over 90 m with low dispersion**
  - 50/125 μm rather than 62.5/125 μm
- **Very little darkening of fiber at HCAL radiation levels (3E11 n/cm2 and 1kRad TID)**
  - Plasma Optical Fiber – Graded-Index Multi-mode (Atlas)
  - CMS HCAL rad test of RM fiber – no measurable change in transmission
- **Controlled environment → No thermal or moisture issues (or rodents!)**



- **Fiber radiation study (Atlas)**
  - Plasma Optic Fiber 50/125μm Graded Index Multi-mode Ge-doped fiber selected
  - Rad Tolerant (~0.1 dB/m at 800 Gy(Si) and 2E13 n/cm^2)

Atlas Liquid Argon Cal (ATL-ELEC-99-001)

Connectors



- **LC / ST**
  - Single-fiber
  - CCM/Calib Patch panels
  - Shutters (LC) Laser safety
- **MTP /MPO**
  - Multi-fiber
  - RMs/HTRs/ Patch panels
  - Shutters – Laser safety

Bit Error Rate Studies

Test 1

- Pedestal data read out of RBX over 50m of cable into a HTR. System clock is ~40Mhz. Commercial PLL at FE. 23 active fibers.
  - BER $<10^{-15}$ over 4 day period

Test 2

- Pedestal data read out of RBX over 50m of cable into a HTR. System clock is ~40Mhz. QPLL used at FE. 12 active fibers.
  - BER $<10^{-15}$ over 4 day period

NOTE – "Dust" test done which showed no increase in these numbers.

Optical Budget Calculation

Power Available	
Minimum transmit power of VCSEL (500uW)	–3 dB
Min Rx Sensitivity at HTR(BER<10^{-12})	–17 dBm
Available Power	14 dB
Power used	
0.1 Km of cable @ 3 dB/Km	0.3 dB
6 or 8 Connectors (includes patch panel)	5.25 dB
LC=0.5dB max, MTP=0.75dB max	
(2LC+4MTP=4.0 dB or 3LC+5MTP = 5.25 dB)	
Typical "Safety Margin"	3.0 dB
Total used	8.55 dB
Excess Power	5.45 dB

Typical Power measured > -7dB

Test Beam 2003 Experience

Test Beam 2003 Experience

- Design is robust
- Operates at speed (1.6Gbps)
- Better design than TB2002 - MTP connectors preferred to SMC
- Modification – Ribbon trunk (female → male)
- Dirt a HUGE issue!
  - Need to get better cleaning tools
    - Cleaning cassettes, alcohol wipes, alcohol swab/stick

Opto-link Design Status

Component Status

- Tested GOL (line-driver) at speed (> 1.6 Gbps) using clean clocks
- Tested Honeywell VCSEL @ at speed
  - Custom packaging
- Tested receivers and de-serializers at speed
- Identified optical connectors and fiber
  - LC simplex and MT multi-way ferrule based connectors
  - Plasma Optical Ge-doped Graded-Index Multimode 50/125 μm fiber
    - Opto-link system budget is driven by fiber cost

Design status

- All link components have been identified
- Identified vendors who can meet our specs
- Tested prototype system at Test Beam 2003 – minor changes needed
- Need final trunk lengths
  - On-detector needed now, off-detector can be later
- Need final TIS approval (Laser safety, materials)

Laser Safety

Hazard classification

- Laser classifications power limits are a strong function of wavelength for reasons of eye focusing effects and the energy of an individual photon
- Initial calculations by TIS laser safety officer
  - VCSEL (850nm) – Class 1 (no restrictions)
    - All individual fibers Class 1
  - Ribbon – Class 1/ Class 3R (signs/labels only)
- Official TIS approval still needed, but opto-link design can accommodate Class 3R classification

Installation Plans

Trunk cable installation

- Dress cables for installation
  - Gang together trunks - reduce cable pulls
  - Special run: 4 16-fiber ribbons (not 2 16-fiber)

Channel mapping verification

- Patch panel/mapping
  - Verify mapping of boxes at Fermilab
  - After installation, verify correct mapping using CCA data transmission (test patterns)

Spares

- Equal length cables – simplify spare situation
  - Patch panel/Fiber storage space is available
- Allowed for 10% spares

Summary and Plans

- **Prototype opto-link system studied at test beam 2003**
  - System can operate at speed
  - System is robust - design problems can be easily addressed
- **Mapping is under control (HCAL)**
- **Fiber plant design nearly complete**
  - Need final trunk lengths (on/off detector)
- **Installation plan is being worked on**
- **Final TIS approval needed soon**